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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-9 (canceled)

Claim 10 (previously presented): An apparatus comprising:

an address multiplexer having a control input;

an address comparator having a received address input, a prefetched address input, and an output coupled to the control input of the address multiplexer; and

an address latch having a first input to accept a prefetched address, a second input to accept a received address, and an address output coupled to a received address input of the address multiplexer to provide the received address to the address multiplexer, wherein the address latch has an output coupled to an enable input of the address comparator to cause the address comparator to be enabled when valid prefetched address data is determined to exist at the first input of the address latch.

Claim 11 (previously presented): An apparatus as defined in Claim 10, wherein the address comparator output is to assume a first value when the received address input is identical to the prefetched address input and to assume a second value when the received address input is not identical to the prefetched address input.

Claim 12 (previously presented): An apparatus as defined in Claim 11, wherein when the address comparator output is the first value, the address multiplexer is to provide the prefetched address to an address multiplexer output.

Claim 13 (previously presented): An apparatus as defined in Claim 11, wherein when the address comparator output is the second value, the address multiplexer is to provide the received address to the address multiplexer output.

Claim 14 (previously presented): An apparatus as defined in Claim 11, wherein the address comparator is enabled only when valid prefetched address data is determined to exist at the prefetched address input of the address comparator.

Claim 15 (previously presented): An apparatus as defined in Claim 14, wherein when the address comparator output is the first value, the address multiplexer is to output the prefetched address.

Claim 16 (previously presented): An apparatus as defined in Claim 14, wherein when the address comparator output is the second value, the address multiplexer is to output the received address.

Claims 17 – 18 (canceled)

Claim 19 (previously presented): An apparatus as defined in Claim 10, wherein the address multiplexer has a first address output coupled to a memory and a second address output coupled to the prefetched address input of the address comparator.

Claim 20 (previously presented): An apparatus as defined in Claim 19, wherein the address comparator output is to assume a first value when the received address input is identical to the prefetched address input and is to assume a second value when the received address input is not identical to the prefetched address input.

Claim 21 (currently amended): A system comprising:

a dynamic prefetch circuit coupled to a memory, the dynamic prefetch circuit comprising:

an address multiplexer having a control input; ~~and~~

an address comparator having a received address input, a prefetched address input, and an output coupled to the control input of the address multiplexer; and

an address latch comprising a first address input to couple to a prefetched address generator, a second address input to couple to a source of received addresses, a first control input to receive a signal to indicate that valid prefetched address data exists at the first address input of the address latch, a second control input to receive a signal to indicate that valid received address data is present at the second address input of the address latch, a clock input coupled to a system clock, and a control output coupled to an enable input of the address comparator to cause the address comparator to be enabled only when valid prefetched address data is determined to exist at the prefetched address input of the address comparator and to cause the address comparator output to change state synchronously with the system clock, and an address output coupled to a received address input of the address multiplexer; and an antenna coupled to the dynamic prefetch circuit.

Claim 22 (previously presented): A system as defined in Claim 21, wherein the address comparator output corresponds to a first value when the received address input is identical to the prefetched address input and corresponds to a second value when the received address input is not identical to the prefetched address input.

Claim 23 (previously presented): A system as defined in Claim 22, wherein when the address comparator output is the first value, the address multiplexer is to output the prefetched address.

Claim 24 (cancel)

Claim 25 (cancel)

Claim 26 (currently amended): A system as defined in Claim [[25]] 21, wherein the address multiplexer has an output coupled to the prefetched address input of the address comparator.

Claims 27 – 30 (canceled)

Claim 31 (currently amended): A method comprising:

comparing a prefetched address with a received address;

providing the prefetched address to a memory to obtain data at the prefetched address within the memory if the comparison is indicative of a match; and

providing the received address to the memory to obtain data at the received address within the memory if the comparison is indicative of a mismatch.

Claim 32 (previously presented): The method of claim 31, further comprising diverting an output of the memory if the comparison is indicative of a mismatch.

Claim 33 (previously presented): The method of claim 31, wherein the prefetched address corresponds to a next address of a burst read operation.

Claim 34 (previously presented): The method of claim 33, further comprising receiving the prefetched address from a read state machine and receiving the received address from a processor.

Claim 35 (previously presented): The method of claim 31, further comprising controlling a multiplexer coupled to the memory based on a result of the comparison.

Claim 36 (previously presented): The method of claim 35, further comprising providing a result of the comparison to the memory via the multiplexer, wherein the memory comprises a non-volatile memory.

Claim 37 (previously presented): The method of claim 35, further comprising providing the prefetched address from the multiplexer to a comparator for the comparison.

Claim 38 (previously presented): The method of claim 31, wherein comparing the prefetched address with the received address comprises comparing a latched prefetch address to the received address.

Claim 39 (previously presented): The method of claim 31, further comprising performing the comparison responsive to completion of a memory address prefetch operation.

Claim 40 (previously presented): A computer-readable medium comprising instructions that, if executed, enable a processor-based system to:

compare a first address with a second address; and

provide the first address to a memory to obtain data at the first address if the comparison is indicative of a match, otherwise to provide the second address to the memory to obtain data at the second address.

Claim 41 (previously presented): The computer-readable medium of claim 40, wherein the instructions enable the processor-based system to perform the comparison responsive to completion of a memory address prefetch operation.

Claim 42 (previously presented): The computer-readable medium of claim 40, wherein the instructions enable the processor-based system to control a multiplexer coupled to the memory based on a result of the comparison.

Claim 43 (previously presented): The computer-readable medium of claim 42, wherein the instructions enable the processor-based system to provide the first address or the second address to the memory via the multiplexer, wherein the memory comprises a non-volatile memory.

Claim 44 (previously presented): The computer-readable medium of claim 40, wherein the first address comprises a prefetched address and the second address comprises an address received from a processor.